

WCH CH340 Series USB Interface Integrated Circuit

CH340G USB to UART Interface Datasheet

WCH Version 1E

DreamCity Version 1.0

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This is a third-party translation of WCH's CH340 Series chipset's Chinese datasheet, with information regarding CH340G chip extracted. The two other chips sharing the same datasheet, CH340R and C340T, have official English version.

1. Overview

CH340 is a series of USB bus adapters, that provides serial, parallel or IrDA interfaces over the USB bus (*note: CH340G supports serial interface only*). The CH340G integrate circuit provides common MODEM signals to allow adding a UART to a computer, or converting existing UART devices to USB interface.

2. Features

- Full-speed USB interface, compatible with USB 2.0 interface.
- Operates with a minimum amount of external components: a crystal and a minimum of four capacitors.
- Provides a virtual serial port for upgrading existing serial port devices or adding serial ports to a PC.
- Supports all existing applications using serial ports without the need of changing existing code.
- Hardware full-duplex serial interface with internal FIFO. Baud rate range from 50bps to 2Mbps.
- Supports common flow control signals RTS, DTR, DCD, RI, DSR and CTS.
- Supports RS232, RS422 and RS485 with external level shifting components.
- Uses CH341 driver.
- Supports 5V and 3.3V operation.
- RoHS-compliant narrow body SO-16 package.

Table of Contents

CH340G USB to UART Interface Datasheet

Disclaimer from DreamCity Innovations	1
1. Overview	1
2. Features	1
Table of Contents	2
3. Specifications	3
3.1. Absolute Maximum Ratings	3
3.2. DC characteristics	3
3.3. AC characteristics	3
4. Pinout	4
5. Application Notes	4
5.1. Example: USB RS232 adapter	5
5.2. Example: Optically isolated USB to UART adapter	6

3. Specifications

3.1. Absolute Maximum Ratings

Operating the chip at or beyond those ratings will cause the chip to malfunction, even irreversibly damage the chip.

Symbol	Name	Minimum	Maximum	Unit
T_A	Operating temperature	-40	85	°C
T_S	Storage temperature	-40	125	°C
V_{CC}	Supply rail voltage, reference to GND pin	-0.5	6.5	V
V_{IO}	IO pin voltage, reference to GND pin	-0.5	$V_{CC}+0.5$	V

3.2. DC characteristics

Symbol	Name	Minimum	Typical	Maximum	Unit
V_{CC}	Supply rail voltage	5V operation	4.5	5	V
		3.3V operation	3.3	3.3	
I_{CC}	Operating current		12	30	mA
I_{SLP}	Sleeping current	5V operation	150	200	μA
		3.3V operation	50	80	
V_{IL}	Low input voltage	-0.5		0.7	V
V_{IH}	High input voltage	2.0		$V_{CC}+0.5$	V
V_{OL}	Low output voltage			0.5	V
V_{OH}	High output voltage	$V_{CC}-0.5$			V
I_{UP}	Internal pull-up strength	3	150	300	μA
I_{DN}	Internal pull-down strength	-50	-150	-300	μA
V_R	Brown-out detector threshold voltage	2.3	2.6	2.9	V

3.3. AC characteristics

Symbol	Name	Minimum	Typical	Maximum	Unit
F_{CLK}	Clock frequency (at pin XI)	11.98	12.00	12.02	MHz
T_{PR}	Power-on reset time		20	50	ms

4. Pinout

Pin #	Name	Direction	Comment
1	GND	Power	Ground reference of the chip. Connect to the ground pin of USB bus.
2	TXD	Output	UART Data Transmit output.
3	RXD	Input	UART Data Receive input.
4	V3	Power	Internal 3.3V reference for USB physical layer. Decouple with a 4.7-20nF capacitor when in 5V operation, or tie to VCC when in 3.3V operation.
5	UD+	Analog	USB D+ signal.
6	UD-	Analog	USB D- signal.
7	XI	Input	Input of the crystal oscillator. Connect to the crystal resonator and load capacitors.
8	XO	Output	Output of the crystal oscillator. Connect to the crystal resonator and load capacitors.
9	CTS#	Input	UART flow control signal Clear to Send.
10	DSR#	Input	UART flow control signal Data Set Ready.
11	RI#	Input	UART flow control signal Ring In.
12	DCD#	Input	UART flow control signal Data Carrier Detect.
13	DTR#	Output	UART flow control signal Data Terminal Ready.
14	RTS#	Output	UART flow control signal Request to Send.
15	R232	Input	Auxiliary RS232 enable. Active high, internal pull down.
16	VCC	Power	Supply rail for the chip.

5. Application Notes

CH340 chip have built in USB bus pull-up resistors and on-chip signal termination, UD+ and UD- pins should be connected to the USB bus lines directly.

CH340 have built in power on reset circuitry.

During operation CH340 requires a 12MHz clock signal present at XI pin. Generally this clock signal is provided by connecting a 12MHz crystal resonator and load capacitors between XI and XO pins, and the built-in crystal resonator will provide the required clock signal. When using an external oscillator feed the clock signal into XI pin, and leave XO pin unconnected.

CH340 supports 5V and 3.3V operation. When using 5V operation, supply 5V to VCC pin, and decouple the internal 3.3V reference with a capacitor of 4.7-20nF from V3 pin to ground. When using 3.3V operation, tie V3 pin to VCC pin and supply 3.3V power.

CH340 supports USB device suspension to reduce energy consumption. When NOS# signal is active this feature is disabled. (*Note: CH340G does not have this pin.*)

Supported hardware flow control signals: CTS#, DSR#, RI#, DCD#, DTR# and RTS#. All flow control pins are software controlled.

Auxiliary pins: IR#, R232, CKO and ACT#. (*Note: only R232 is present on CH340G*) When R232 signal is asserted the RXD signal is inverted. R232 is latched during Power-On Reset.

By adding infrared adapters, CH340 can be used to implement USB to SIR adapter, allowing a PC to communicate with IrDA peripheral.

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DreamCity Innovations Page 6 of 6 WCH CH340G Datasheet